ADJUSTABLE PHASE CONTROLLED CLOCK AND DATA RECOVERY CIRCUIT

Abstract

A clock and data recovery circuit including: means for generating a first and a second clock signal; means for receiving the first clock signal and for generating a third clock signal from the first clock signal and means for receiving the second clock signal and for generating a fourth clock signal, wherein at least one of the third and the fourth clock signals differ in phase from the first and the second clock signal respectively; means for receiving the third and fourth clock signals and a serial data stream and for generating a reconstructed serial data stream and a phase error signal; means for receiving the phase error signal and for generating a phase adjustment signal and means for receiving the phase adjustment signal by the by the clock generation circuit in a feedback loop to adjust the phases of the first and second clock signals.